XR-1096

Graphic Equalizer Filter and Display Driver

...the analog plus company™

September 1996-4

FEATURES

- Simple Resistor and Capacitor Oscillator
- Provides Seven Filters and Display Multiplexer In One
- DIM Pin for Controlling Display Brightness
- Peak Holding Delay Control With a Resistor and a Capacitor
- Dual Inputs for Summing Left and Right Channels
- Provides 30 dB of Gain
- Low Noise CMOS

APPLICATIONS

- Graphic Equalizers
- Tape Recorders
- Receivers
- Portable Systems
- Spectrum Analysis

GENERAL DESCRIPTION

The XR-1096 is a switched-capacitor filter, multiplexer and high voltage driver dedicated for use in audio applications to perform the band splitting function and vacuum florescent display driver. The XR-1096 contains seven band-pass filters spaced 1.32 octaves apart from 63 Hz to 16kHz followed by seven analog peak detectors. A digital peak detect is also provided for the total output which is an indication of the maximum signal level within the range of the band-pass filters. Two separate inputs allow the left and right channels to be summed. This reduces the display space and prevents redundant information in the audio from being displayed.

The internal band-pass filters and peak detect circuits of the XR-1096 have low output offset voltage to prevent false displays from occurring during the playback of low volume music or music with wide dynamic range. The nominal operating voltages are ±5VDC. The self contained oscillator is designed to operate at 400 kHz with an external resistor and capacitor.

The output multiplexer is designed to interface with most vacuum florescent display drivers having up to 13 steps for level and seven frequency bands. The total output is also provided for displays with this band as well. The high voltage P-channel driving transistors in the XR-1096 have a maximum drain to source voltage of -40V.

The XR-1096 is fabricated in 3 µm double polysilicon CMOS for lower noise and less clock feedthrough in the internal stages and is available in a 32 pin shrink DIP plastic package.

ORDERING INFORMATION

Part No.	Package	Operating Temperature Range
XR-1096CP	32 Lead 400 Mil SDIP	-30°C to 75°C

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BLOCK DIAGRAM

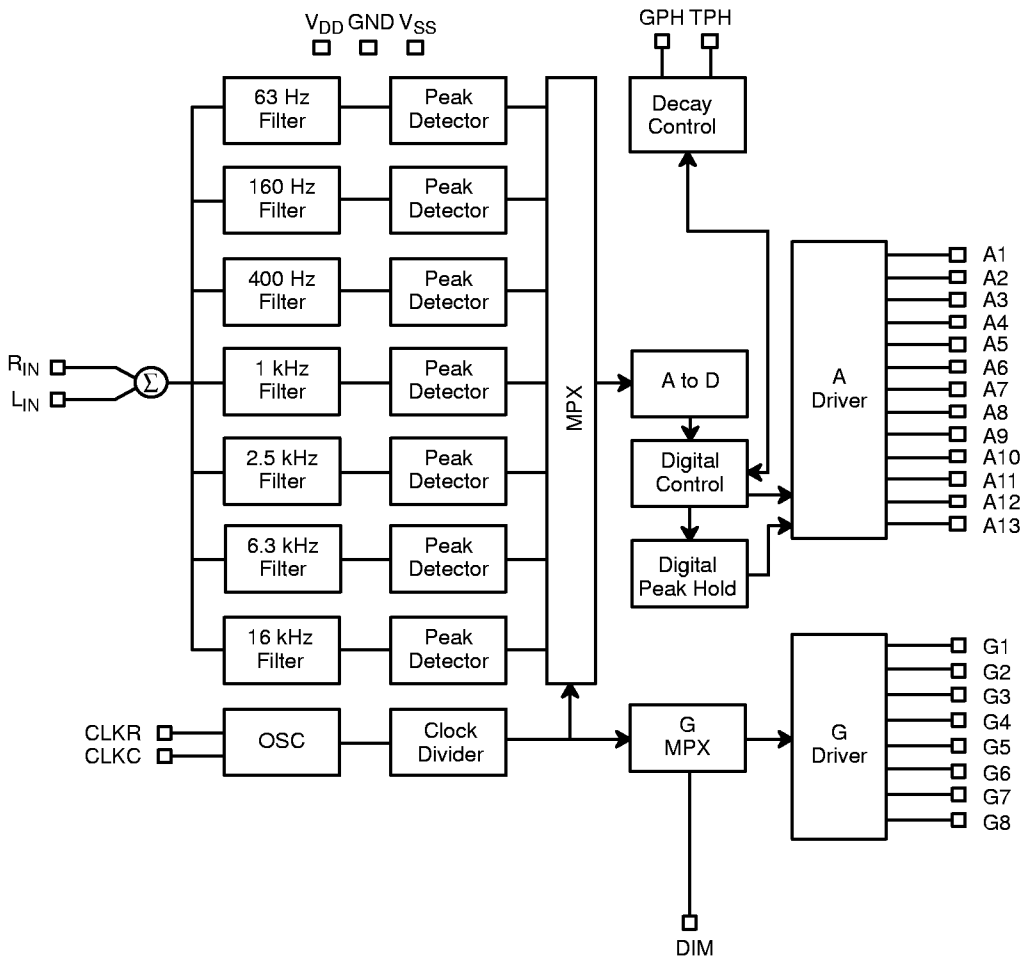
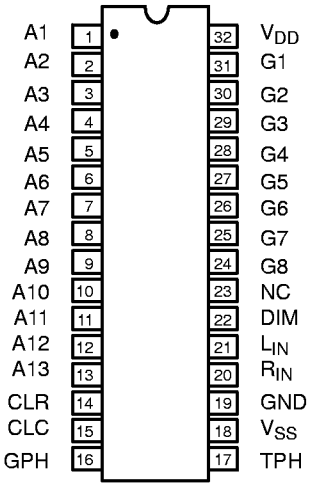


Figure 1. Block Diagram

PIN CONFIGURATION



32 Lead SDIP (0.400")

PIN DESCRIPTION

Pin #	Symbol	Description
1-13	A1-A13	Amplitude levels 1-13: This indicates the signal strength.
14	CLKR	Clock resistor: The timing resistor would be tied from this pin to pin 15, CLKC.
15	CLKC	Clock capacitor: The timing capacitor should be tied from this pin to V_{SS}.
16	GPH	A resistor and a timing capacitor from this pin to V_{SS} will control the duration the display bands are peak held.
17	TPH	A resistor and a timing capacitor from this pin to V_{SS} will control the duration the total output is peak held.
18	V_{SS}	Nominally -5VDC.
19	GND	Ground: Should be tied to a low impedance ground line.
20	R_{IN}	Right Channel Input
21	L_{IN}	Left Channel Input
22	DIM	Dim Display: This pin, when high, reduces the brightness of the display by adjusting the on time of the segments.
23	NC	No internal connection.
24-31	G8-G1	Time allocation for different frequency bands. See table below:
		G1 63 Hz
		G2 160 Hz
		G3 400 Hz
		G4 1 kHz
		G5 2.5 kHz
		G6 6.3 kHz
		G7 16 kHz
		G8 Total Output
		e.g. when G1 is high (V_{DD}), data at A1-A13 is for 63Hz signals.
32	V_{DD}	Nominally tied to +5VDC.

ELECTRICAL CHARACTERISTICS

Test Conditions: V_{DD} = +5V, V_{SS} = -5V, V_D = -33 V, T_A = 25°C, unless otherwise specified.

Symbol	Parameter	Min.	Typ.	Max.	Unit	Conditions
I_{DD5}	Supply Current		15	20	mA	V_{DD} = 5VDC, V_{SS} = -5VDC
I_{IL}	Input Leakage	-2		2	µA	L_{IN}, R_{IN}, DIM, CLC
TCLKRP (R-C)	Clock Freq Accuracy	375	400	425	kHz	R = 1.46kΩ, C = 1n
f_o	Filter Freq Accuracy	-7	0	7	%	
I OFF	All A outputs off			10	µA	V_{IN} = 0V, V_D = -35 V
V_{OUT} G	All G outputs	-1.0	2.5	5	V	V_{DD} = 5V I_{GL} = 14mA
V_{OUT} A	All A outputs	2.5	3.75	5	V	V_{DD} = 5V I_{AL} = 2.5mA
T_D	Output Decay Time		330		ms	
t_d	Duty Cycle		1/11.4			
t_f	Duty Factor		833		µs	With DIM at V_{SS}
			240		µs	With DIM at V_{DD}
TPH	Total Hold Time		0.5		s	R = 100KΩ, C = 1µf
GPH	Individual f_c hold time		0.5		s	R = 100KΩ, C = 1µf
Amplitude Test Limits[1]						
A1	–30dB	5.8	7.7	8.5	mVpk	
A2	–28dB	8.5	9.5	10.7	mVpk	
A3	–26dB	10.7	12.0	13.5	mVpk	
A4	–24dB	13.5	16.0	18.0	mVpk	
A5	–22dB	18.0	20.0	22.5	mVpk	
A6	–20dB	22.5	25.5	28.5	mVpk	
A7	–18dB	28.5	32.5	35.5	mVpk	
A8	–16dB	35.5	41.0	45.5	mVpk	
A9	–14dB	45.5	50.5	57.0	mVpk	
A10	–12dB	57.0	64.0	70.0	mVpk	
A11	–10dB	70.0	77.0	89.0	mVpk	
A12	–8dB	89.0	102.0	116	mVpk	
A13	–4dB	116	127	150	mVpk	

Notes

[1]Amplified levels are relative to V_{DD} at 5 volts nominal. Levels will vary linearly with voltage on V_{DD}.

Specifications are subject to change without notice

ABSOLUTE MAXIMUM RATINGS

V_{DD} 7VDC
V_{SS} ..... -7VDC
VDS of High Voltage P-Channel Driving Transistors:
Relative to V_{DD} ..... - 45 V
Power Dissipations (package limitation) .....
32 Pin Plastic Package ..... 1 W
Derate above 25°C ..... 9 mW/°C
Storage Temperature ..... -60°C to +150°C

SYSTEM DESCRIPTION

The XR-1096, unlike most switched-capacitor filters, does not require an external clock source in order to provide the sampling clock. This frees the designer to place the XR-1096 in any application where an active filter design was in place. The XR-1096 provides filters at 63 Hz, 160 Hz, 400 Hz, 1kHz, 2.5 kHz, 6.3 kHz, and 16 kHz. These frequencies are relative standards in the consumer audio market. The display decoder is designed for use with vacuum florescent displays and provides the control expected in such a multiplexer. These include dimming of the display's brightness and delay for peak hold of all 8 bands (7 frequency bands and 1 total output).

The XR-1096 contains a continuous-time anti-aliasing filter. This prevents out of band signals from affecting the filters performance. If two separate displays are desired, then two XR-1096 could be used, and the unused input should be grounded.

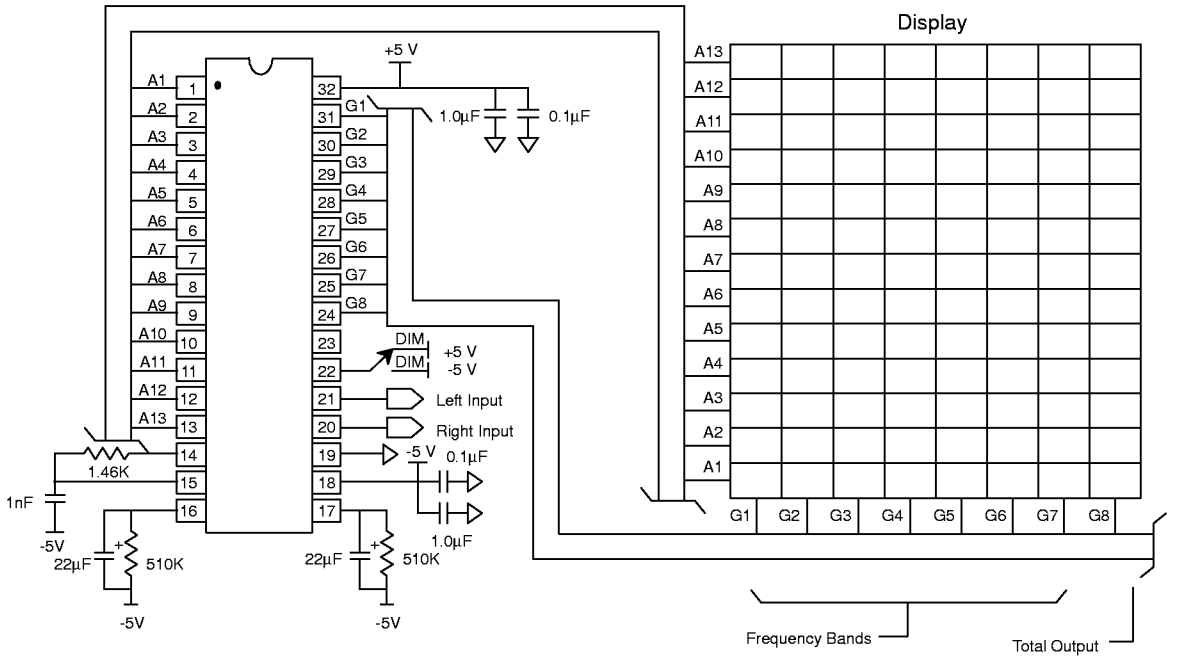
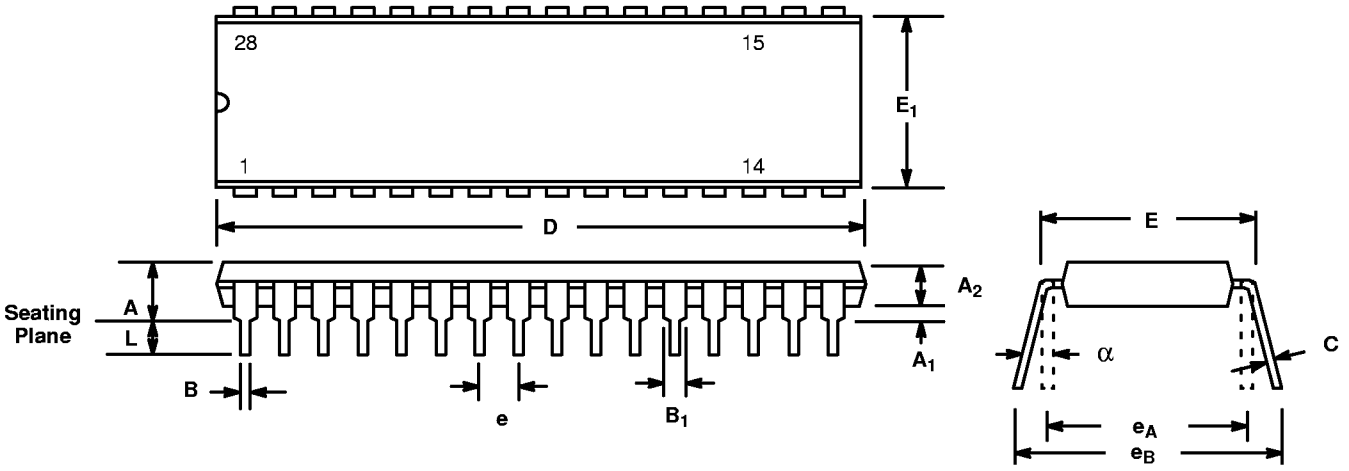


Figure 2. Typical Application Schematic

32 LEAD SHRINK PLASTIC DUAL-IN-LINE (400 MIL SDIP)

Rev. 1.00



SYMBOL	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	0.140	0.200	3.56	5.08
A_1	0.020	0.070	0.51	1.78
A_2	0.120	0.180	3.05	4.57
B	0.014	0.023	0.35	0.59
B_1	0.030	0.055	0.75	1.42
C	0.008	0.014	0.20	0.36
D	1.080	1.120	27.43	28.45
E	0.390	0.435	9.91	11.05
E_1	0.300	0.370	7.62	9.40
e	0.070 BSC		1.78 BSC	
e_A	0.400 BSC		10.16 BSC	
e_B	0.400	0.500	10.16	12.70
L	0.100	0.150	2.54	3.40
α	0°	15°	0°	15°

Note: The control dimension is the inch column